

# Kevin L. Seaman

<https://www.linkedin.com/in/KevinLSeaman>

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## PROFILE: SR. PRINTED CIRCUIT BOARD CAD ENGINEER

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- Senior CAD Engineer with 50+ years in PCB Design, Electromechanical Packaging, PCB CAD, and Programming.
- Accomplished in effectively contributing to all phases of PCB product development from conception to post sales customer support, including 10 years of PCB Library and Database Management and 5 years of Pre/Post Sales CAD Technical Support.
- Excellent verbal and written communication skills, problem-solving creativity, and the ability to deliver innovative solutions to resolve continually changing, and often challenging, technical obstacles.
- Cultivates productive relationships with clients and cross-functional teams while expertly integrating client requirements with engineering and manufacturing capabilities and limitations.
- Co-authored 6 US Patents on BGA Routing Depopulation Optimization and published an article in PC Design Magazine.

### Core Competencies & Technical Skills

Printed Circuit Board Design: HDI Type 3 & 4 (2.5 mils) ♦ Substrates (25 microns) ♦ Interposers (2 microns)

Cross-functional Team Leadership ♦ PCB Library & Database Management

Pre/Post Sales CAD Technical Support ♦ Electromechanical Packaging ♦ Valor ♦ CAM ♦ DFM ♦ DFA

Cadence Allegro ♦ Cadence OrCAD CIS Capture ♦ Cadence Concept ♦ PCB Librarian ♦ Database Management

Microsoft: Excel, Access, Word, PowerPoint, Outlook ♦ Programming/Coding: PHP, JavaScript, SQL, UNIX, C, CAD, DOS

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## PROFESSIONAL EXPERIENCE

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**NORTHROP GRUMMAN | OCT 2023 – PRESENT** (temporary contract)

### SR PCB DESIGNER

- ♦ Utilized Cadence Allegro 17.4 to Design Class 3 PC Boards.

**MERCURY SYSTEMS, INC | MAY 2021 – AUG 2023**

### PRINCIPAL CAD ENGINEER

- ♦ Utilized Cadence Allegro 17.4 & 22.2 to Design Interposers, Substrates, and HDI Type 3 & 4 PC Boards.

**GENERAL DYNAMICS | OCT 2017 – MAY 2021** (temporary contract to permanent employee)

### SR. PC BOARD DESIGNER / LIBRARY SUPPORT / VALOR QA OPERATOR

- ♦ Utilized Cadence Allegro and Mentor Xpedition to Design HDI Type 3 & 4 PC Boards. Interim Cadence and Mentor Librarian.

**INTEL CORPORATION | SEP 2017 – OCT 2017** (temporary contract)

### CAD DESIGNER

- ♦ Utilized Cadence Allegro 17.2 for Design of HDI Type 3 & 4 PC Boards.

**FREEDOM CAD SERVICES INC | FEB 2017 – SEP 2017** (temporary contract)

### PC BOARD DESIGNER / VALOR QA OPERATOR / LIBRARY SUPPORT

- ♦ Utilized Cadence Allegro 16.6/17.2 for PC Board Design, Valor QA, and Library support.

## PROFESSIONAL EXPERIENCE (continued)

### BROADCOM CORPORATION | APR 1999 – DEC 2016

#### PC BOARD DESIGNER, PRINCIPAL / ORCAD CAPTURE CIS LIBRARIAN / VALOR QA OPERATOR / PROGRAMMER

- ♦ Utilized Cadence Allegro for PCB Design of HDI, Multi-Layer, Micro-Via, SMT, Digital/Analog/RF PC Boards for product test, characterization, and high-volume production. Wrote macros to enhance and automate CAD tools.
- ♦ Delivered on-time designs of up to five simultaneous boards utilizing in-house and outside resources.
- ♦ Led development of a PHP/JavaScript Intranet GUI to document the scope of individual PC Board designs which then dynamically created a Status and Check List unique to each board, all visible to Engineering. Managed a support team of twelve designers to effectively contribute to the GUI content and functionality ultimately yielding higher quality designs and fewer Valor QA passes.
- ♦ Co-authored 6 US patents for optimizing BGA depopulation enabling high pin count devices to be routed using fewer signal layers.

### ROCKWELL / CONEXANT | 1991 – APR 1999

#### SR. CAD PCB DESIGNER / PCB LIBRARIAN

- ♦ Utilized Cadnetix and DDE Supermax E-CAD in Schematic Capture and Design of High-Density, Multi-Layer, Micro-Via PC Boards. Developed libraries and wrote macros to enhance and automate CAD tools.

#### PRIOR EXPERIENCE:

Sr. CAD PCB Designer / System Administrator in Orange & San Diego Counties, CA & Phoenix, AZ

Sr. CAD Application Engineer at Mentor Graphics Corporation, Mission Viejo, CA

Sr. CAD Application Engineer at Cadnetix/Dazix Corporation, Mesa, AZ & Newport Beach, CA

## EDUCATION & PROFESSIONAL TRAINING

Certified Interconnect Designer (CID) - IPC ♦ CAD Tools - Cadence, Mentor, DDE, Cadnetix, Calma

UNIX, C, and Windows Graphics Programming - University of California Irvine, CA ♦ HTML Web Pages - Saddleback Community College, CA

Electronics & BASIC Programming - Rio Salado Community College, AZ ♦ High School Graduate - Saguaro High School, Scottsdale, AZ

## PATENTS & PUBLICATIONS

#### PATENTS:

- ♦ US Patent 8,695,212 Method for optimizing routing layers and board space requirements for a ball grid array land pattern, **Apr 2014**
- ♦ US Patent 7,855,448 Optimization of routing layers and board space requirements for ball grid array package implementations including array corner considerations, **Dec 2010**
- ♦ US Patent 7,816,247 Optimization of routing layers and board space requirements for ball grid array package implementations including array corner considerations, **Oct 2010**
- ♦ US Patent 7,009,115 Optimization of routing layers and board space requirements for a ball grid array package, **Mar 2006**
- ♦ US Patent 7,005,753 Optimization of routing layers and board space requirements for a ball grid array land pattern, **Feb 2006**
- ♦ US Patent 6,916,995 Optimization of routing layers and board space requirements for ball grid array package implementations including single and multi-layer routing, **Jul 2005**

#### PUBLICATIONS:

- ♦ RS-274-X Gerber File Format, PC Design Magazine, **Mar 1996**